SGS-THOMSON MICROELECTRONICS

M27C516

512K (32K x 16) OTP EPROM

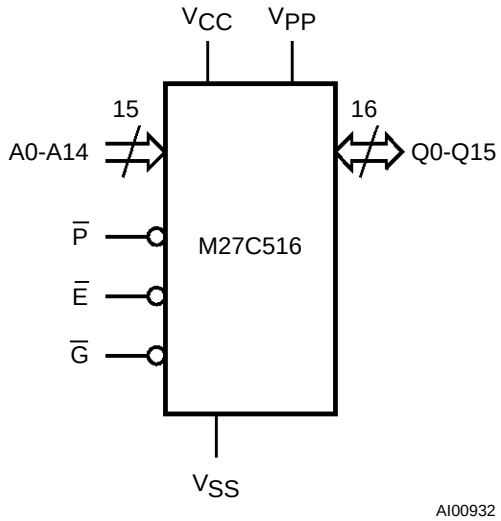
PRODUCT PREVIEW

- FAST ACCESS TIME: 45ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 3sec. (PRESTO II ALGORITHM)

PLCC44 (C)

TSOP40 (N)
10 x 14mm

Figure 1. Logic Diagram



DESCRIPTION

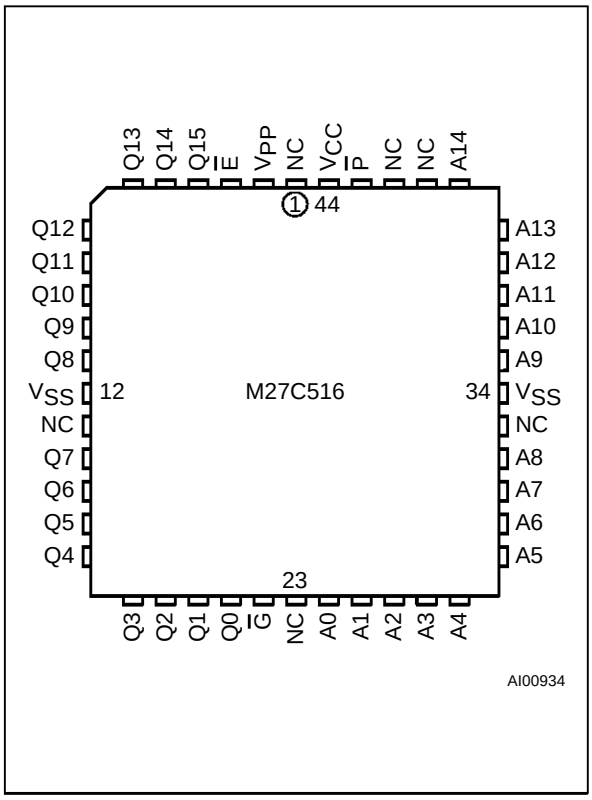
The M27C516 is an high speed 512K bit One Time Programmable EPROM ideally suited for handheld and portable microprocessor systems requiring large program. It is organized as 32,768 by 16 bits.

For equipment requiring a surface mounted, low profile package, the M27C516 is offered in a Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

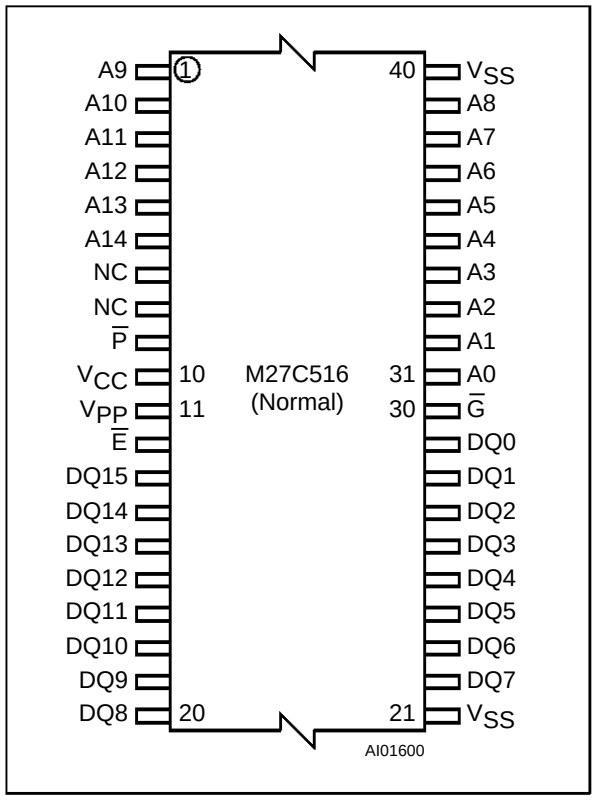
A0 - A14	Address Inputs
Q0 - Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program Enable
V_{CC}	Supply Voltage
V_{PP}	Program Supply
V_{SS}	Ground

Figure 2A. LCC Pin Connections



Warning: NC = Not Connected

Figure 2B. TSOP Pin Connections



Warning: NC = Not Connected

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9}	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q15
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	Hi-Z
Program	V_{IL}	X	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	1	1	1	1	0Fh

DEVICE OPERATION

The modes of operations of the M27C516 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27C516 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C516 has a standby mode which reduces the active current from 35mA to 100µA. The M27C516 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because OTP EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Table 5. AC Measurement Conditions

	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 20ns
Input Pulse Voltages	0 to 3V	0.4V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

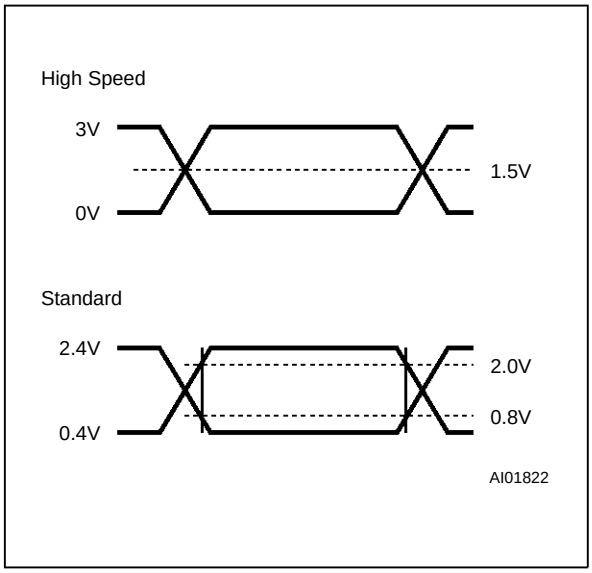


Figure 4. AC Testing Load Circuit

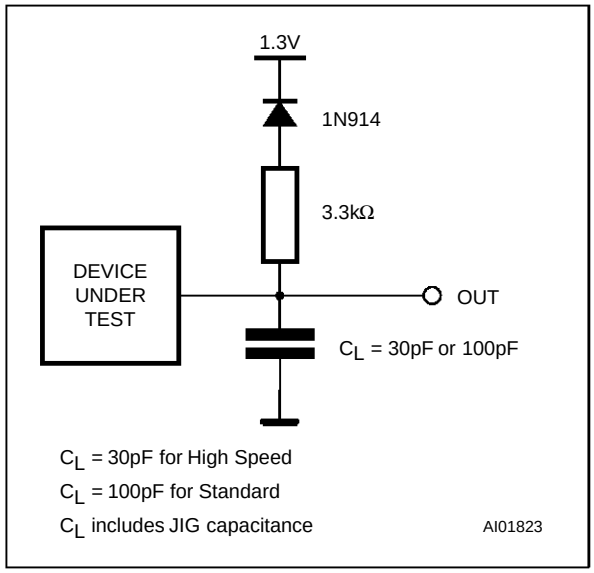


Table 6. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. This parameter is sampled only and not tested 100%.

System Considerations

The power switching characteristics of Advanced CMOS OTP EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 7. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} – 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 8A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C516								Unit
				-45 (3)		-70		-90		-10		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		45		70		90		100	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		45		70		90		100	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		25		35		45		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	20	0	25	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	20	0	25	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

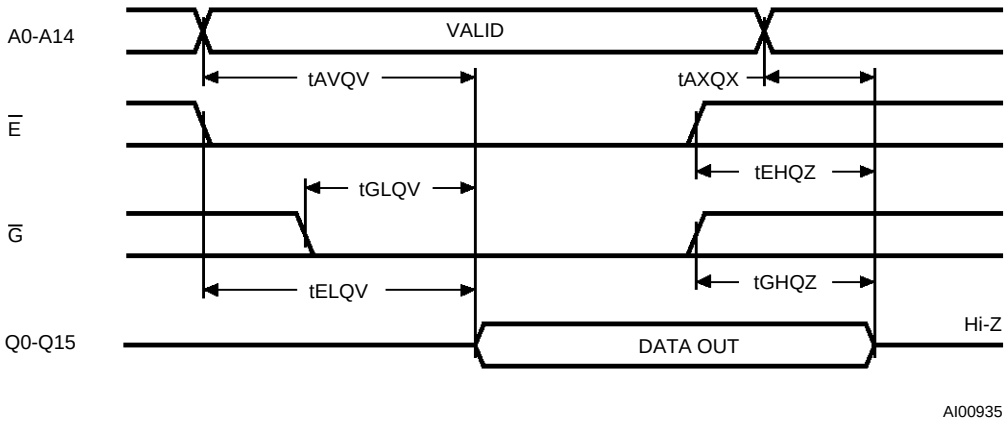
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. Sampled only, not 100% tested.
3. In case of 45ns speed see High Speed AC measurement conditions.

Table 8B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C516						Unit
				-12		-15		-20		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	50	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms



Programming

When delivered, all bits of the M27C516 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word. The M27C516 is in the programming mode when V_{PP} input is at 12.75V, $\overline{E}$ is at V_{IL} and $\overline{P}$ is pulsed to V_{IL}. The data to be programmed is applied to 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ±0.25V.

Table 9. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		µs

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

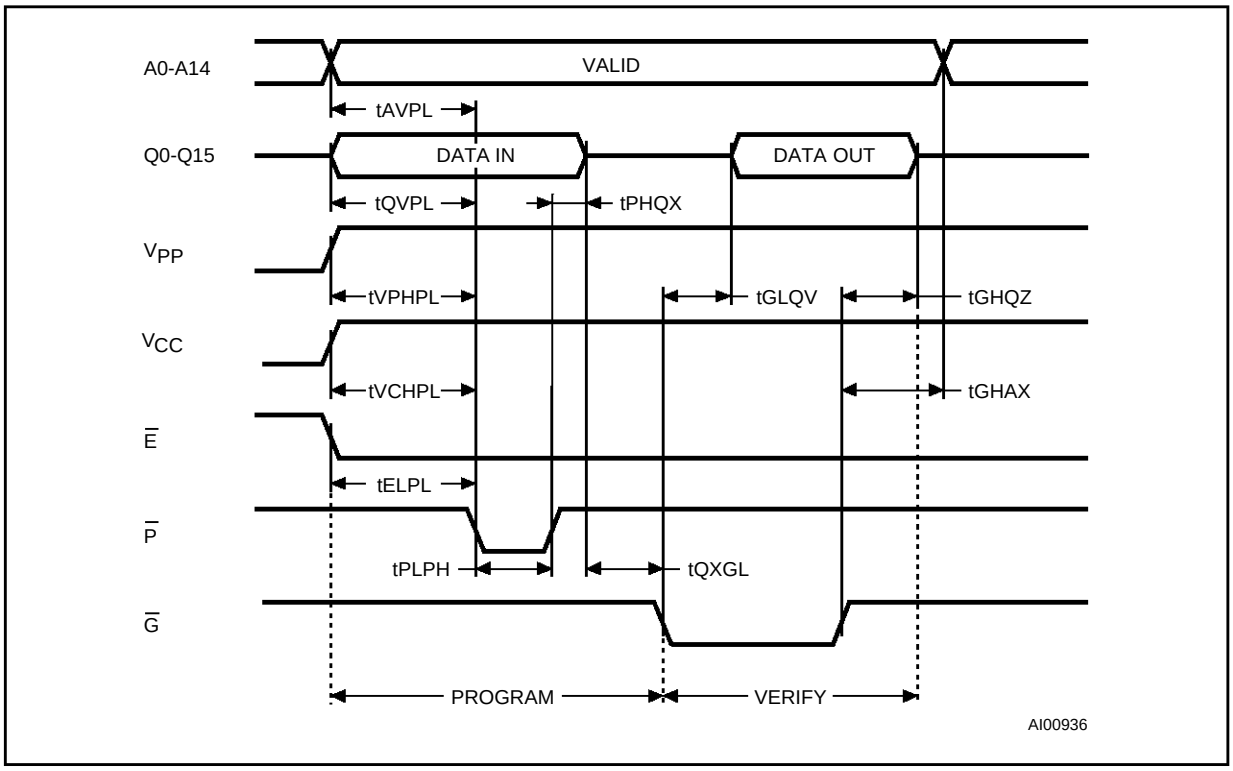
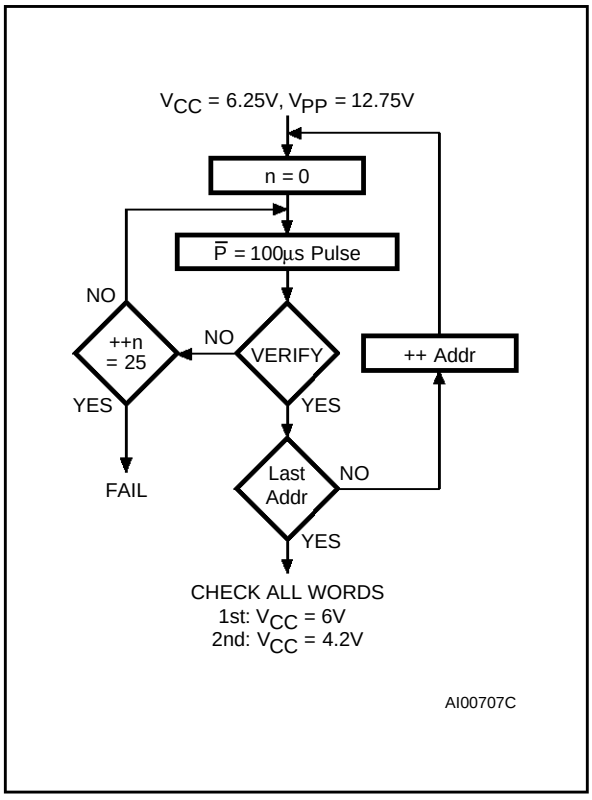


Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of 3 seconds. Programming with PRESTO II involves the application of a sequence of 100µs program pulses to each byte until a correct verify occurs (see Figure 7). During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C516s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C516 may be common. A TTL low level pulse applied to a M27C516's $\overline{P}$ input, with $\overline{E}$ low and V_{PP} at 12.75V, will program that M27C516. A high level $\overline{E}$ input inhibits the other M27C516s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

On-Board Programming

The M27C516 can be directly programmed in the application circuit. See the relevant Application Note AN620.

Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an OTP EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C516. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C516.

Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C516, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ORDERING INFORMATION SCHEME

Example: M27C516 -70 X N 1 TR

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-45 (1)	45 ns	X	±5%	C	PLCC44	1	0 to 70 °C	TR	Tape & Reel Packing
-70	70 ns	blank	±10%	N	TSOP40 10 x 14mm	6	–40 to 85 °C		
-90	90 ns								
-10	100 ns								
-12	120 ns								
-15	150 ns								
-20	200 ns								

Note: 1. High Speed, see AC Characteristics section for further information.

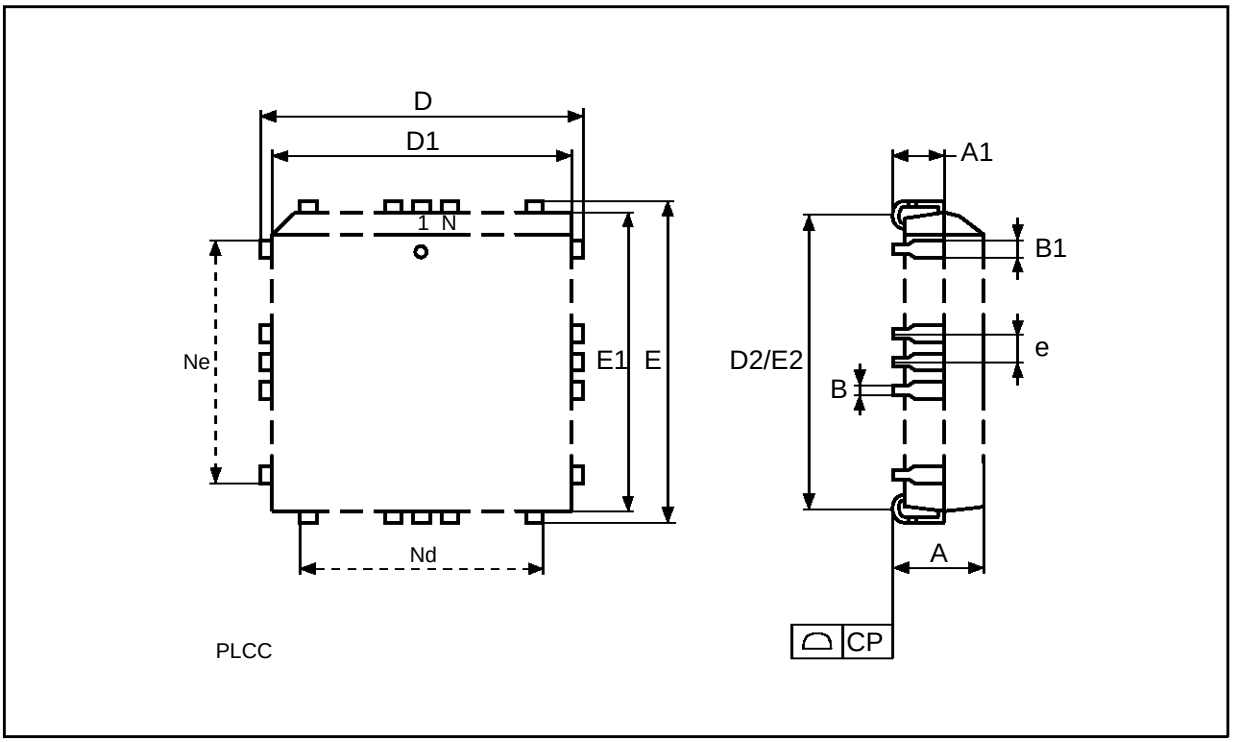
For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PLCC44 - 44 lead Plastic Leaded Chip Carrier, square

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		4.20	4.70		0.165	0.185
A1		2.29	3.04		0.090	0.120
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		17.40	17.65		0.685	0.695
D1		16.51	16.66		0.650	0.656
D2		14.99	16.00		0.590	0.630
E		17.40	17.65		0.685	0.695
E1		16.51	16.66		0.650	0.656
E2		14.99	16.00		0.590	0.630
e	1.27	–	–	0.050	–	–
N	44			44		
CP			0.10			0.004

PLCC44



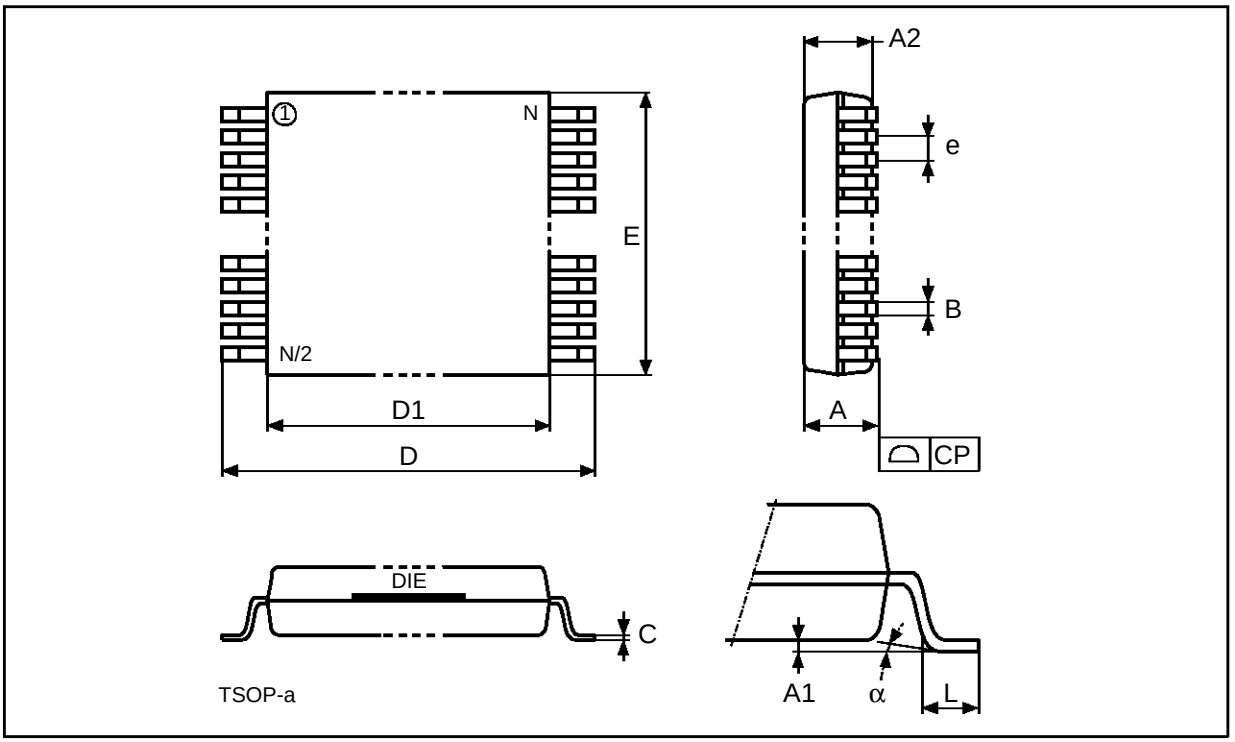
PLCC

Drawing is not to scale

TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 14mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.80	14.20		0.543	0.559
D1		12.30	12.50		0.484	0.492
E		9.90	10.10		0.390	0.398
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	40			40		
CP			0.10			0.004

TSOP40



TSOP-a

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